AN10765

P89LPC9351/9321 migration

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Document information

Info	Content
Keywords	LPC9351, LPC9321, LPC935, LPC932A1, Migration
Abstract	This application note covers the important features that were added to the P89LPC9351/9321. These features should be considered when migrating from the P89LPC935/932A1.

Revision history

Rev	Date	Description
01	20081201	First version

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1. Introduction

This document provides information regarding the migration of the P89LPC935/932A1 to the P89LPC9351/9321 This document should be used in conjunction with the device datasheet. The following is a list of the differences between the two microcontrollers.

The followed aspects are covered in this document:

1. Pinning
2. Reset
3. Memory
4. Clock
5. Brownout detection
6. ADC functions (LPC9351 only)
7. Analog comparators
8. Readable RTC
9. User configuration bytes
10. Power consumption
11. Difference in Keil IDE
12. IAP/ISP mode
13. Parallel programming

2. Pinning

The pinning of both micros are the same. Compared with the P89LPC935/932A1, the P89LPC9351/9321 has eight I/O pins with high current sourcing/sinking (20 mA). These eight I/O pins include P0.3 to P0.7, P1.4, P1.6 and P1.7.

3. Memory

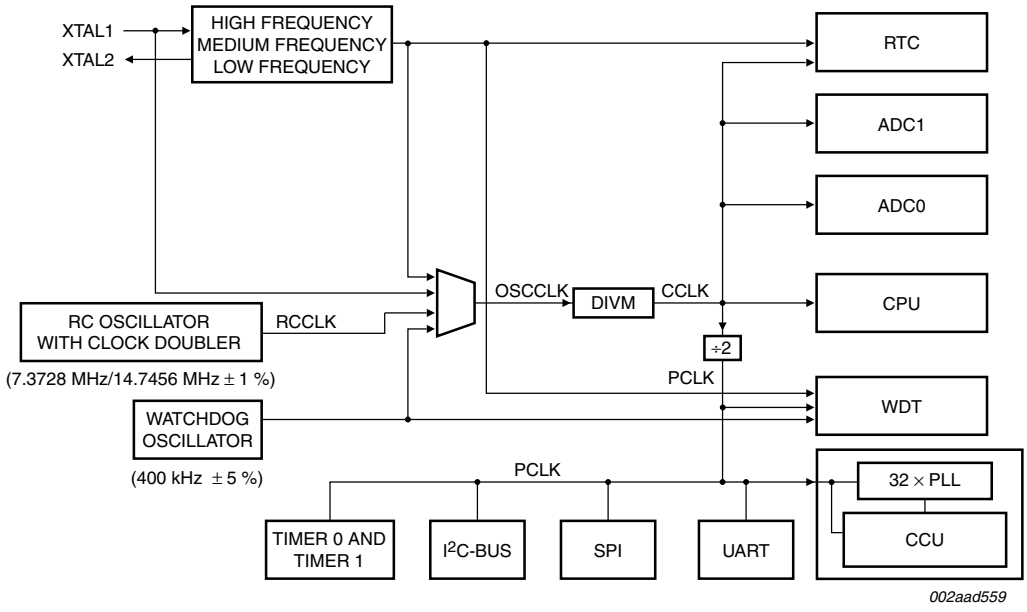
The memory maps of both microcontrollers are the same.

4. Reset

In the P89LPC9351/9321, a watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.

5. Clocks

Fig 1 gives the block diagram of oscillator control of the P89LPC9351/9321.



(1) A series resistor may be required to limit crystal drive levels. This is especially important for low frequency crystals (see text)

Fig 1. Block diagram of oscillator control

5.1 Clock doubler option

In the P89LPC9351/9321, the internal RC oscillator has a clock 'doubler' option. UCFG2.7 is used to control the clock doubler option. When set, it doubles the output frequency of the internal RC oscillator to 14.746 MHz. The unprogrammed value of UCFG2.7 is zero, disabling the clock double option.

5.2 Watchdog oscillator option

Both the P89LPC935/932A1 and the P89LPC9351/9321 have a watchdog oscillator of 400 kHz. In the P89LPC9351/9321, the accuracy of the watchdog oscillator has been improved to ±5% at room temperature.

5.3 WDT clock source

In the P89LPC935/932A1, the WDT can be clocked from the watchdog oscillator and PCLK. In the P89LPC9351/9321, the external crystal oscillator can also be the clock source of the WDT. XTALWD bit in the CLKCON register is used to configure this feature. When '1', the external crystal oscillator is chosen to be the clock source of the WDT. When '0', the clock source configuration of WDT is the same with P89LPC935/932A1. The reset value of XTALWD bit is '0'.

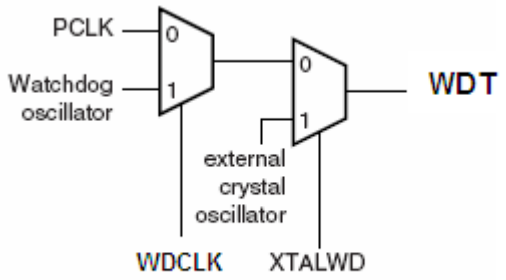


Fig 2. WDT clock source

5.4 Clock switching on the fly

A new feature called 'clock switch on the fly' is added to the P89LPC9351/9321.

It can implement clock source switching on any sources of watchdog oscillator, 7/14MHz IRC oscillator, external crystal oscillator and external clock input during code is execution. The CLKCON register is used to control this function. During reset, the CLKCON register value comes from UCFG1 and UCFG2.

Please see the P89LPC9351/9321 UM and AN of clock source switching on the fly for more detailed information.

6. Brownout detection

In the P89LPC935/932A1, Brownout detection can be configured to cause a processor reset or to generate an interrupt. BOE (UCFG1.5), BOPD (PCON.5) and PMOD1/PMOD0 (PCON[1:0]) are used to enable brownout detection. BOI (PCON.4) is used to switch between brownout detection reset and interrupt.

Compared with the P89LPC935/932A1, the P89LPC9351/9321 has enhanced brownout detection, including 3 independent functions: BOD reset, BOD interrupt and BOD EEPROM/FLASH.

BOD reset will cause a processor reset and it is always enabled, except in total power-down mode. BOD interrupt will generate an interrupt and can be enabled or disabled in software.

For BOD reset and BOD interrupt, each has 4 trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of the BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt.

BOD EEPROM/FLASH is used for flash/Data EEPROM program/erase protection. The BOD EEPROM/FLASH has only 1 trip voltage level of 2.4V. The EWERR1 and EWERR0 bits in the DEECON register are used to indicate the write error of the BOD EEPROM.

Please see the P89LPC9351/9321 UM section 6.1 Brownout detection and Section 18 Data EEPROM and AN of enhanced BOD function of the LPC9351 for more information.

7. ADC functions (LPC9351 only)

In the P89LPC9351, the ADC function has been enhanced. Two high-speed programmable gain amplifiers (PGA) and an on-chip temperature sensor are integrated. The block diagram of ADC is shown in Fig 3.

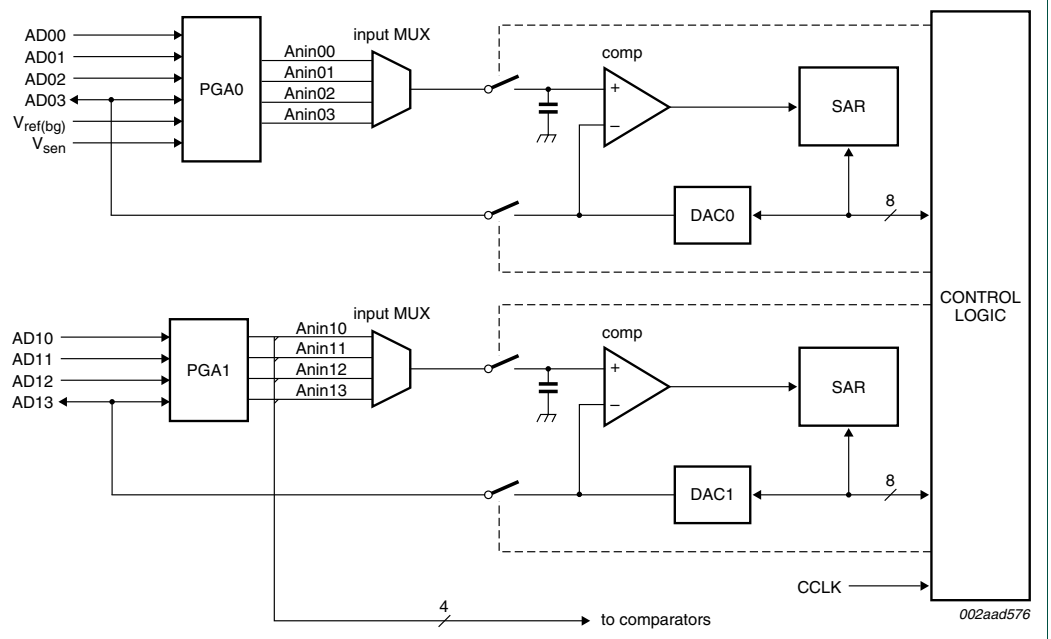


Fig 3. ADC block diagram

Two 8-bit ADCs are integrated. The conversion speed of the ADC has been improved to 8-bit conversion time of ≥1.61 μs at an A/D clock of 8.0 MHz.

In each ADC module, a PGA module is integrated to improve the effective resolution of the ADC. A single channel can be selected for amplification. The gain of the PGA can be programmed to 2x, 4x, 8x and 16x. An on-chip wide-temperature range temperature sensor is integrated with the ADC0 module. It provides temperature sensing capability between −40 °C ~ 85 °C. The registers PGACONx and PGACONxB are used for the PGA and temperature sensor configuration. The reset value of the PGA control register is '0' which means the PGA and the temperature sensor are both disabled.

Please see the P89LPC9351 UM, AN of how to use LPC9351 PGA and AN of how to use LPC9351 temperature sensor for more information.

If the PGAs, temperature sensor or the A/D are enabled, they will consume power. Power can be reduced by disabling the PGA, temperature sensor and A/D. In Power-down mode or Total Power-down mode, the A/D, PGA and temperature sensor do not function.

8. Analog comparators

In the LPC9351/9321, the comparators inputs can also be amplified by PGA1. This is configured by programming the registers PGACON1 and PGACON1B. The reset value of PGA1 control registers is '0' which means PGA1 is disabled.

9. Readable RTC

In the P89LPC9351/9321, the 16-bit counter portion of the RTC is readable by accessing the RTCDATH and RTCDATL registers. Please see AN of LPC9351 readable RTC for more detailed information..

10. User configuration bytes

In the P89LPC9351/9321, two user configuration bytes are used for user-configurable features. In UCFG1, UCFG1.5 and UCFG1.3 are used as BOD reset trip point configuration bits. But in the P89LPC935/932A1, UCFG1.5 is used for Brownout Detect Enable and UCG1.3 is reserved.

The Clock doubler option of internal RC oscillator is configured by bit UCFG2.7 in the P89LPC9351/9321.

The factory preprogrammed value of UCFG1 and UCFG2 is 0x63 and 0x00 respectively. This means the trip voltage of BOD reset is 2.4V,and the CPU clock source is the internal RC oscillator of 7.373MHz.

Please refer to the P89LPC9351/9321 UM for details.

Table 1. Flash User Configuration Byte 1 (UCFG1) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WDTE	RPE	BOE1	WDSE	BOE0	FOSC2	FOSC1	FOSC0
Unprogrammed value	0	1	0	0	0	0	1	1

Table 2. Flash User Configuration Byte 2 (UCFG2) bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	CLKDBL	-	-	-	-	-	-	-
Unprogrammed value	0	X	x	x	x	x	x	x

11. Power consumption

Compared with the LPC935/932A1, the LPC9351/9321 achieves lower power consumption in power down mode.

With external crystal option, the LPC9351 can implement 32 KHz WDT. Lower power consumption can be achieved.

Table 3. P89LPC9351/9321 $I_{DD(pd)}$ and $I_{DD(tpd)}$, V_{DD} = 3.3 V, T_{amb} = 25 °C

Parameter	Test Condition	Min	Typ	Max	Unit
$I_{DD(pd)}$ Power-down mode supply current	Using IRC with the following functions disabled: comparators, real-time clock and watchdog timer.		20		µA
	Using IRC with the following functions disabled: comparators, real-time clock. 32KHz watchdog timer enabled.		38		µA
$I_{DD(tpd)}$ Total Power-down mode supply current	Using IRC with the following functions disabled: comparators, brownout detect, real-time clock and watchdog timer.		0.5		µA
	Using IRC with the following functions disabled: comparators, brownout detect, real-time clock. 32KHz watchdog timer enabled.		20		µA
	Using IRC with the following functions disabled: comparators, brownout detect. 32KHz watchdog timer and 32KHz real-time clock enabled.		22		µA

Please refer to P89LPC9351/9321 DS for details.

12. Difference in Keil IDE

The definition of User configuration bytes may be different according to the part number of LPC900. So it's better to use configuration wizard to edit START900.A51 in Keil IDE.

To implement this, first find the option for the LPC9351/9321 and then configure UCFG1, UCFG2 and so on according to users' application. Fig 4 gives Keil uVision3 editor window.

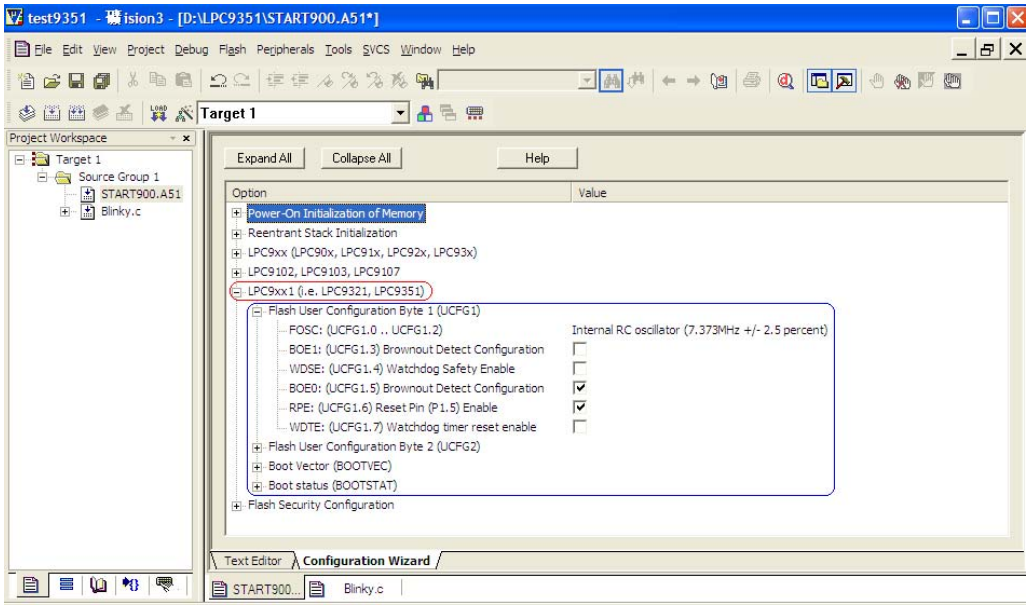


Fig 4. Keil uVision3 editor window

13. ISP/IAP mode

The ISP/IAP mode of the P89LPC9351/9321 is the same as that of the P89LPC935/932A1.

14. Parallel programming

The P89LPC9351/9321 can be programmed using the same algorithm as the P89LPC935/932A1.

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